ABSTRACT

Double buffering of serial transfers is provided in order to allow for increased serial transfer rate without requiring increased internal processing speeds. A serial controller serially receives a word including address bits and data bits. During a write operation, the address bits are serially shifted into an address shift register, and the data bits are serially shifted into a data shift register. After the address bits and data bits are completely shifted into the respective address and data shift registers, the address bits and data bits are transferred in parallel to address and data holding registers. After the parallel transfers of the address bits and data bits from the address and data shift registers to the address and data holding registers, the address and data shift registers are available to serially receive additional address bits and data bits of an additional word.